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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,350	08/02/2001	Edson W. Porter	01-050 1496.00128	6030

24319 7590 08/13/2004

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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,350	PORTER ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-20* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/30/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 20 are presented for examination.

Claim Objections

2. Claim 9 is objected to because of the following informalities:

3. In the claim 9, the term " ISI " needs an abbreviation at least once in claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 – 20 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Kuo, US Patent 6,377,095.

6. As to claim 1, Kuo discloses an apparatus [differential line driver, fig. 1] and method [for controlling rise and fall time] [for controlling rise and fall time] comprising:

a. a first plurality of parallel switches [N parallel driver cells as in fig. 3, each having MA, MB, as in fig.5] configured control a voltage [by turning on and off transistors with controlled current and delay time] on a first output pin [D+] ; and

b. a second plurality of parallel switches [N parallel driver cells as in fig. 3, each having MNA, MNB, as in fig.5] configured to control a voltage [by turning on and off transistor with controlled current and delay time] on a second output pin [D-], wherein said first [N parallel

driver cells as in fig. 3, each having MA, MB, as in fig.5] and second [N parallel driver cells as in fig. 3, each having MNA, MNB, as in fig.5] pluralities of parallel switches are configured to provide rise time control [controlling rise and fall time] of a differential waveform [D+, D-] and are driven by [N parallel drivers] phased data signal [DATA_IN] [col. 1, lines 6 – 8, lines 53 – 67, col. 2, lines 1 – 67, col. 3, lines 1 – 51, col. 4, lines 12 – 61, fig.1, 3, and 5 – 6].

7. As to claim 19, Kuo discloses an apparatus [differential line driver, fig. 2] and method [for controlling rise and fall time] [for controlling rise and fall time] comprising:

a. means [driver circuit] for controlling a voltage [by turning on and off transistors with controlled current and delay time] on a first output pin [D+] with a first plurality of parallel switches [N parallel driver cells as in fig. 3, each having MA, MB, as in fig.5];

b. means [driver circuit] controlling a voltage [by turning on and off transistors with controlled current and delay time] on a second output pin [D-] with a second plurality of parallel switches [N parallel driver cells as in fig. 3, each having MNA, MNB, as in fig.5]; and

c. means [bias circuit] for providing rise time control [controlling rise and fall time] of a differential waveform [D+, D-], wherein first [N parallel driver cells as in fig. 3, each having MA, MB, as in fig.5] and second pluralities of parallel switches [N parallel driver cells as in fig. 3, each having MNA, MNB, as in fig.5] are driven by [N parallel drivers] a phased data signal [DATA_IN] [col. 1, lines 6 – 8, lines 53 – 67, col. 2, lines 1 – 67, col. 3, lines 1 – 51, col. 4, lines 12 – 61, fig. 1, 3, and 5 – 6].

8. As to claim 20, Kuo discloses an apparatus [differential line driver, fig. 1] and method [for controlling rise and fall time] comprising:

(A) controlling a voltage [by turning on and off transistors with controlled current and delay time] on a first output pin [D+] with a first plurality of parallel switches [switches as shown 210, 224 in fig.2, and 230 in fig. 5];

(B) controlling a voltage [by turning on and off transistors with controlled current and delay time] on second output pin [D-] with a second plurality of parallel switches [N parallel driver cells as in fig. 3, each having MNA, MNB, as in fig.5]; and

(C) providing rise time control [controlling rise and fall time] of a differential waveform [D+, D-], wherein said first [N parallel driver cells as in fig. 3, each having MA, MB, as in fig.5] and second pluralities of parallel switches [N parallel driver cells as in fig. 3, each having MNA, MNB, as in fig.5] are driven by [N parallel drivers] a phased data signal [DATA_IN] [col. 1, lines 6 – 8, lines 53 – 67, col. 2, lines 1 – 67, col. 3, lines 1 – 51, col. 4, lines 12 – 61, fig. 1, 3, and 5 – 6].

9. As to claim 2, Kuo discloses a first [rising] and last phase [falling] of phased data signal [DATA_IN] is configured to determine a rise and fall time [by determining current level bias] of differential wave form [D+, D-][col. 2, lines 56 – 67, col. 3, lines 1 – 36].

10. As to claim 3, Kuo discloses a first [MA, MB] and second [MNA, MNB] pluralities of parallel switches [in N parallel drivers] are weighed [by controlled current] to determine a pulse shape [by determining the current level bias] of differential wave form [D+, D-] [col. 1, lines 5 – 14, fig. 3].

11. As to claims 4, 5, and 6, Kuo discloses one or more sources [IS1, IS2, fig. 9] parallel and configured to provide current to each of first and second pluralities of parallel switches and current sources are weighed [by controlled current] to determine a pulse shape [by determining

the current level bias] of differential wave form [D+, D-] [col. 1, lines 5 – 14, fig. 3] [col. 3, lines 17 – 41, fig. 3, 6, 9].

12. As to claim 7, Kuo discloses a first driver configured in parallel; and second driver configured in parallel, wherein said first and second drivers are configured to synchronize to a phased clock signal [CLOCK][col. 5, lines 33 – 53] [fig. 1 - 3].

13. As to claim 8, Kuo discloses first [data shaper] and second [edge rate control logic] drivers configured to perform pre-emphasis [reshapes based upon clock] on differential waveform [col. 1, lines 5 – 14, fig. 1, 3].

14. As to claim 9, as Kuo discloses an apparatus [differential line driver] to drive differential signal with drivers [N parallel drivers] and driver bias circuit [BIAS circuit] to control the current with mirrored current technique to generate differential output which inherently teaches to mitigate the ISI effects [glitches][col. 3, lines 46 – 52].

15. As to claim 10, Kuo discloses first driver [data shaper] comprises a main driver and second driver [edge rate control logic] comprises a secondary driver [N parallel driver] [fig. 3].

16. As to claim 11, Kuo discloses first driver [data shaper] and second driver [edge rate control logic] comprises one or more flip-flops [latches][fig. 3].

17. As to claim 12, Kuo discloses first and second drivers clocked by [CLOCK] a multiphase [inherent property of clock signal] clock signal [fig. 3].

18. As to claims 13, and 14, Kuo discloses a clock [data clock] generation signal [D+, D-] configured to generate multiphase clock [D+, D-] in response to a data signal [D1, D2] and a precompensation signal [PBIAS1, PBIAS2][fig. 1 - 3].

19. As to claim 16, Kuo discloses generation of first phase [D+] and second phase [D-] are controlled by a bias [PBIAS1, PBIAS2][fig. 1 - 3].

20. As to claim 17, Kuo discloses that an apparatus [differential line driver] is configured to overcome cable induced [glitch] effects [col.3, lines 48 – 52].

21. As to claim 18, Kuo discloses an apparatus [differential line driver] configured to synchronize [by producing a first and second control signals skewed in time by a time delay] a plurality of drivers to provide precompensation [col. 4, lines 19 – 30].

22. Claims 1 – 20 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Groen, US Patent 6,437,599.

23. As to claim 1, Groen discloses an apparatus [200, fig. 2] and method comprising:

a. a first plurality of parallel switches [switches as shown 210, 224 in fig.2, and 230 in fig. 5] configured control a voltage [by turning on and off transistors] on a first output pin [205, out+] ; and

b. a second plurality of parallel switches [switches as shown 220, 226 in fig. 2, and 230 in fig. 5] configured to control a voltage [by turning on and off transistors] on a second output pin [203, OUT-], wherein said first [switches as shown 210, 224 in fig.2, and 230 in fig. 5] and second [switches as shown 220, 226 in fig. 2, and 230 in fig. 5] pluralities of parallel switches are configured to provide rise time control [it is inherent to electrical property of current, voltage, and time relationship that the rise time or slew rate (i.e. output reaches amplitude) varies proportionate to the rate in change of current flow, please refer to cited references] of a differential waveform [out+, out-] and are driven by [drivers 210, 220] phased

data signal [204, in+, 202, in-] [col. 2, lines 54 – 67, col. 3, lines 1 – 31, col. 4, lines 22 – 65][fig.2 – 5].

24. As to claim 19, Groen discloses an apparatus [200, fig. 2] and method comprising:

a. means [210, driver circuit] for controlling a voltage [by turning on and off transistors] on a first output pin [205] with a first plurality of parallel switches [switches as shown 210, 224 in fig.2, and 230 in fig. 5];

b. means [220, driver circuit] controlling a voltage [by turning on and off transistors] on a second output pin [203] with a second plurality of parallel switches [switches as shown 220, 226 in fig. 2, and 230 in fig. 5]; and

c. means [230, driver bias circuit] for providing rise time control [it is inherent to electrical property of current, voltage, and time relationship that the rise time or slew rate (i.e. output reaches amplitude) varies proportionate to the rate in change of current flow, please refer to cited references] of a differential waveform [out+, out-], wherein first [switches as shown 210, 224 in fig.2, and 230 in fig. 5] and second pluralities of parallel switches [switches as shown 220, 226 in fig. 2, and 230 in fig. 5] are driven by [drivers 210, 220] a phased data signal [204, in+, 202, in-] [col. 2, lines 54 – 67, col. 3, lines 1 – 31, col. 4, lines 22 – 65, col. 4, lines 14 - 21][fig.2 – 5].

25. As to claim 20, Groen discloses an apparatus [200, fig. 2] and method comprising:

(A) controlling a voltage [by turning on and off transistors] on a first output pin [205, out+] with a first plurality of parallel switches [switches as shown 210, 224 in fig.2, and 230 in fig. 5];

(B) controlling a voltage [by turning on and off transistors] on second output pin [203, out-] with a second plurality of parallel switches [switches as shown 220, 226 in fig. 2, and 230 in fig. 5]; and

(C) providing rise time control [it is inherent to electrical property of current, voltage, and time relationship that the rise time or slew rate (i.e. output reaches amplitude) varies proportionate to the rate in change of current flow, please refer to cited references] of a differential waveform [out+, out-], wherein said first [switches as shown 210, 224 in fig.2, and 230 in fig. 5] and second pluralities of parallel switches [switches as shown 220, 226 in fig. 2, and 230 in fig. 5] are driven by [drivers 210, 220] a phased data signal [204, in+, 202, in-] [col. 2, lines 54 – 67, col. 3, lines 1 – 31, col. 4, lines 22 – 65, col. 4, lines 14 - 21][fig.2 – 5].

26. As to claim 2, Groen discloses a first [rising] and last phase [falling] of phased data signal [204, in+, 202, in-] is configured to determine a rise and fall time [by determining current level bias] of differential wave form [at 203, 205][col. 3, lines 31 – 39].

27. As to claim 3, Groen discloses a first [switches as shown 210, 224 in fig.2, and 230 in fig. 5] and second pluralities of parallel switches [switches as shown 220, 226 in fig. 2, and 230 in fig. 5] are weighed [by mirrored current] to determine a pulse shape [by determining the current level bias] of differential wave form [at 203, 205] [col. 3, lines 31 – 39, col. 4, lines 14 – 40, fig. 2 - 5].

28. As to claims 4 – 6 Groen discloses an apparatus [200, fig. 2] with a bias driver circuit [230] that controls [as shown in fig.2 – 5] the bias currents of driver circuits [210, 220] with an arrangements for providing current to each of first [via itop_main, ibot_main, ibias_vref] and second pluralities of parallel switches [via itop_emp, ibot_emp, ibias_vref] and weighed [by

current mirrored] to determine a pulse shape [by determining the current level bias] of differential wave form [at 203, 205] [col. 3, lines 31 – 39, col. 4, lines 14 – 40, fig. 2 - 5].

29. As to claim 8, Groen discloses first [210] and second [220] drivers configured to perform pre-emphasis on differential waveform [col. 2, lines 59 – 62, fig. 2].

30. As to claim 9, as Groen teaches an apparatus [200] to drive differential signal with drivers [210, 220] and driver bias circuit [230] to control the current with mirrored current technique to generate differential output which inherently teaches to mitigate the ISI effects [rise time and fall time effects][col. 4, lines 14 – 38, fig. 2-5].

31. As to claim 10, Groen discloses first driver [210] comprises a main driver [main driver] and second driver [220] comprises a secondary driver [emphasis circuit][fig. 2][col. 2, lines 59 – 62, fig. 2].

Allowable Subject Matter

32. Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 703-305-3994. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 703-308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
August 9, 2004